

DATA SHEET

74F657

Octal transceiver with 8-bit parity
generator/checker

Product data
Supersedes data of 1990 Jul 30

2003 Feb 04

Octal transceiver with 8-bit parity generator/checker

74F657

FEATURES

- Combines 74F245 and 74F280A functions in one package
- High impedance base input for reduced loading (70 μ A in HIGH and LOW states)
- Ideal in applications where high output drive and light bus loading are required (I_{IL} is 70 μ A versus FAST std of 600 μ A)
- 3-state buffer outputs sink 64 mA and source 15 mA
- Input diodes for termination effects
- 24-pin plastic slim DIP (300 mil) package
- Industrial temperature range available (-40°C to $+85^{\circ}\text{C}$)

DESCRIPTION

The 74F657 is an octal transceiver featuring non-inverting buffers with 3-state outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 24 mA at the A ports and 64 mA at the B ports. The transmit/receive (T/R) input determines the direction of the data flow through the bidirectional transceivers.

Transmit (active HIGH) enables data from A ports to B ports; receive (active LOW) enables data from B ports to A ports.

The output enable ($\overline{\text{OE}}$) input disables both the A and B ports by placing them in a high impedance condition when the $\overline{\text{OE}}$ input is HIGH.

The parity select (ODD/EVEN) input gives the user the option of odd or even parity systems.

The parity (PARITY) pin is an output from the generator/checker when transmitting from the port A to B ($T/\overline{R}$ = HIGH) and an input when receiving from port B to A port ($T/\overline{R}$ = LOW).

When transmitting ($T/\overline{R}$ = HIGH) the parity select (ODD/EVEN) input is set, then the A port data is polled to determine the number of high bits. The parity (PARITY) output then goes to the logic state determined by the parity select (ODD/EVEN) setting and by the number of high bits on port A.

For example, if the parity select (ODD/EVEN) is set LOW (even parity), and the number of high bits on port A is odd, then the parity (PARITY) output will be HIGH, transmitting even parity. If the number of high bits on port A is even, then the parity (PARITY) output will be LOW, keeping even parity.

When in receive mode ($T/\overline{R}$ = LOW) the B port is polled to determine the number of high bits. If parity select (ODD/EVEN) is LOW (even parity) and the number of highs on port B is:

(1) odd and the parity (PARITY) input is HIGH, then $\overline{\text{ERROR}}$ will be HIGH, significantly no error.

(2) even and the parity (PARITY) input is HIGH, then $\overline{\text{ERROR}}$ will be asserted LOW, indicating an error.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F657	8.0ns	100 mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5\text{ V} \pm 10\%$, $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$	INDUSTRIAL RANGE $V_{CC} = 5\text{ V} \pm 10\%$, $T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	
24-pin plastic slim DIP (300 mil)	N74F657N	I74F657N	SOT222-1
24-pin plastic SOL	N74F657D	I74F657D	SOT137-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH / LOW	LOAD VALUE HIGH / LOW
A0–A7	A ports 3–state inputs	3.5 / 0.117	70 μ A / 70 μ A
B0–B7	B ports 3–state inputs	3.5 / 0.117	70 μ A / 70 μ A
PARITY	Parity input	3.5 / 0.117	70 μ A / 70 μ A
T/ $\overline{R}$	Transmit/receive input	2.0 / 0.066	40 μ A / 40 μ A
ODD/EVEN	Parity select input	1.0 / 0.033	20 μ A / 20 μ A
$\overline{\text{OE}}$	Output enable input (active LOW)	2.0 / 0.066	40 μ A / 40 μ A
A0–A7	A ports 3–state outputs	150 / 40	3.0 mA / 24 mA
B0–B7	B ports 3–state outputs	750 / 106.7	15 mA / 64 mA
PARITY	Parity output	750 / 106.7	15 mA / 64 mA
$\overline{\text{ERROR}}$	Error output	750 / 106.7	15 mA / 64 mA

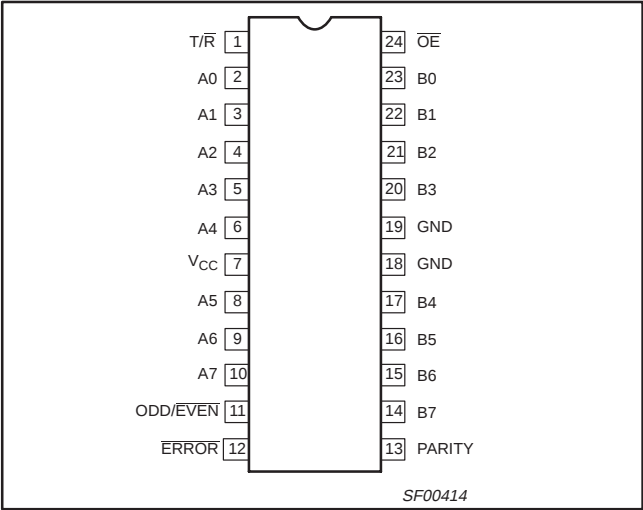
NOTE:

1. One (1.0) FAST unit load is defined as: 20 μ A in the HIGH state and 0.6 mA in the LOW state.

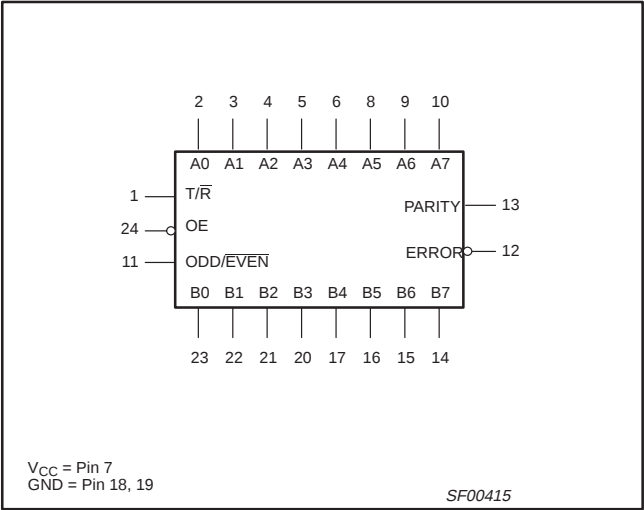
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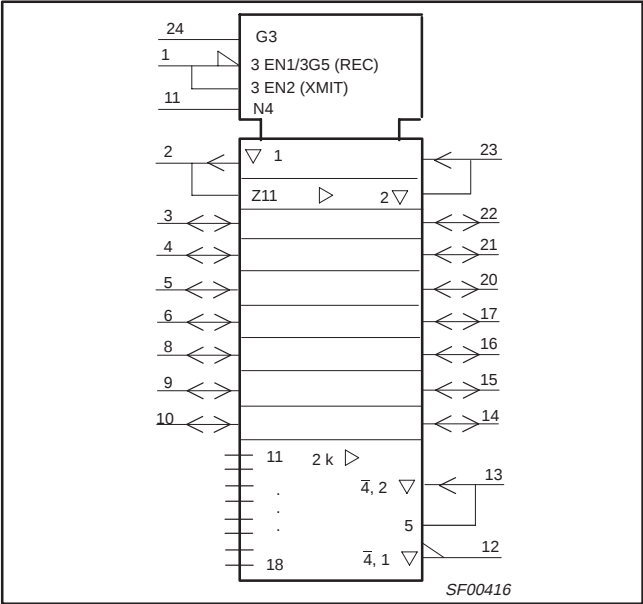
PIN CONFIGURATION



LOGIC SYMBOL



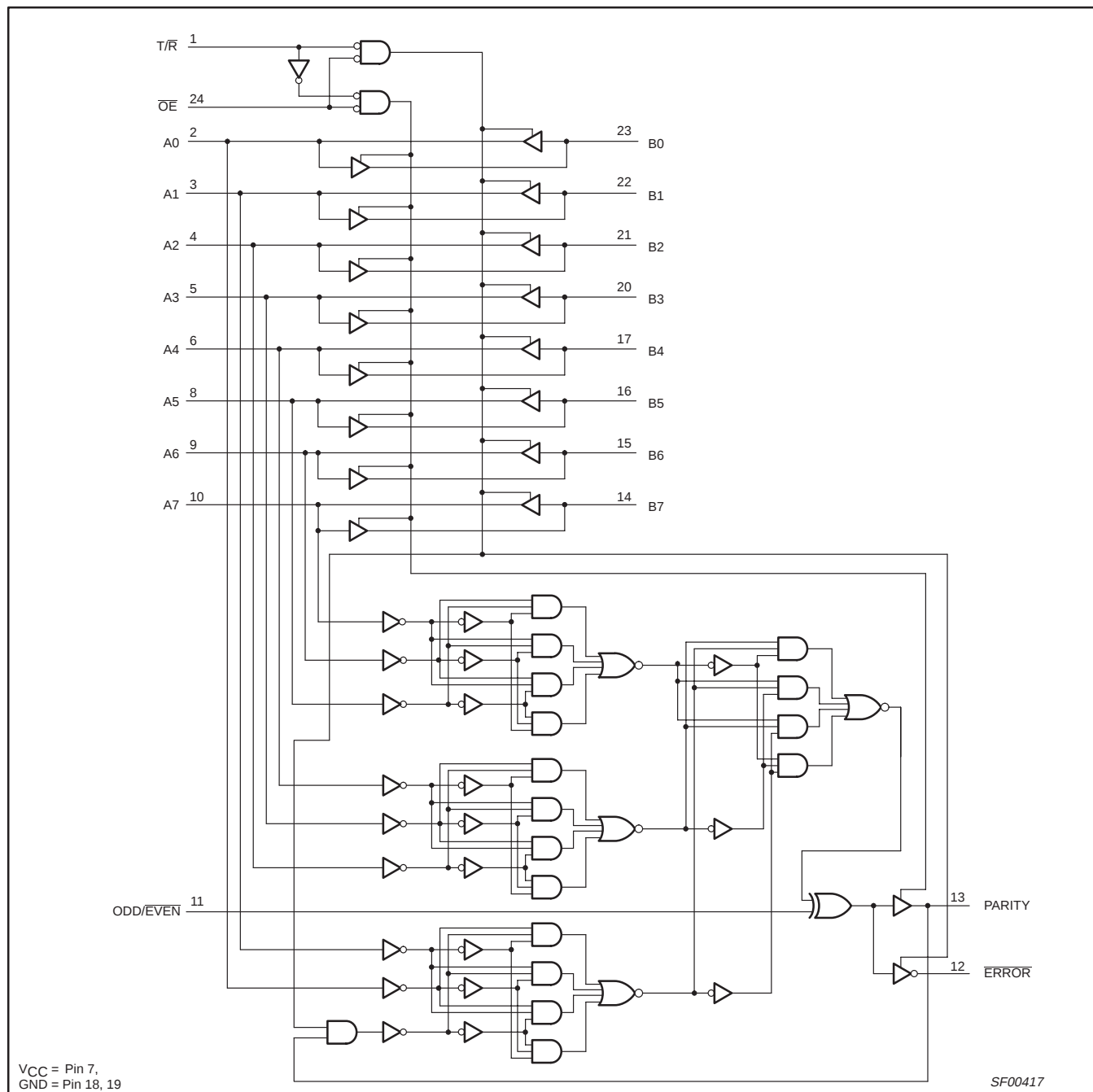
IEC/IEEE SYMBOL



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LOGIC DIAGRAM



Octal transceiver with 8-bit parity generator/checker

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FUNCTION TABLE

NUMBER OF INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT	OUTPUTS	
	OE	T/R	ODD/EVEN	PARITY	ERROR	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

Notes to function table

1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limit set forth in this table may impair the useful life of the device.

Unless otherwise noted these limits are over the operating free air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V _{CC}	Supply voltage		−0.5 to +7.0	V
V _{IN}	Input voltage		−0.5 to +7.0	V
I _{IN}	Input current		−30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state		−0.5 to V _{CC}	V
I _{OUT}	Current applied to output in LOW output state	A0–A7	48	mA
		B0–B7, PARITY, ERROR	128	mA
T _{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	−40 to +85	°C
T _{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5.0	5.5	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage				0.8	V
I _{IK}	Input clamp current				−18	mA
I _{OH}	HIGH-level output current	A0–A7			−3	mA
		B0–B7, PARITY, ERROR			−15	mA
I _{OL}	LOW-level output current	A0–A7			24	mA
		B0–B7, PARITY, ERROR			64	mA
T _{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	−40		+85	°C

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS ¹			LIMITS			UNIT
						MIN	TYP ²	MAX	
V _{OH}	HIGH-level output voltage	All outputs	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = −3 mA ^{4,5}	±10%V _{CC}	2.4			V
		±5%V _{CC}			2.7			V	
		B0–B7, PARITY, ERROR		I _{OH} = −12 mA ⁵	±10%V _{CC}	2.0			V
					±5%V _{CC}	2.0			V
				I _{OH} = −15 mA ⁴	±10%V _{CC}	2.0			V
					±5%V _{CC}	2.0			V
V _{OL}	LOW-level output voltage	A0–A7	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = 24 mA ^{4,5}	±10%V _{CC}		0.35	0.50	V
		±5%V _{CC}				0.35	0.50	V	
		B0–B7, PARITY, ERROR		I _{OL} = 48 mA ⁴	±10%V _{CC}		0.38	0.55	V
					±5%V _{CC}		0.42	0.55	V
				I _{OL} = 48 mA ⁵	±5%V _{CC}		0.42	0.55	V
					I _{OL} = 64 mA ⁴	±5%V _{CC}		0.42	0.55
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}				−0.73	−1.2	V
I _I	Input current at maximum input voltage	$\overline{\text{OE}}$, T/ $\overline{\text{R}}$, ODD/EVEN	V _{CC} = 0.0 V, V _I = 7.0 V					100	μA
		A0–A7	V _{CC} = 5.5 V, V _I = 5.5 V					2	mA
		B0–B7						1	mA
I _{IH}	HIGH-level input current	ODD/ $\overline{\text{EVEN}}$	V _{CC} = MAX, V _I = 2.7 V					20 ⁴	μA
							40 ⁵	μA	
		$\overline{\text{OE}}$, T/ $\overline{\text{R}}$						40 ⁴	μA
							80 ⁵	μA	
I _{IL}	LOW-level input current	OOD/ $\overline{\text{EVEN}}$	V _{CC} = MAX, V _I = 0.5 V					−20	μA
		$\overline{\text{OE}}$, T/ $\overline{\text{R}}$						−40	μA
I _{OZH} + I _{IH}	Off-state output current, HIGH-level voltage applied	A0–A7, B0–B7, PARITY	V _{CC} = MAX, V _O = 2.7 V					70	μA
I _{OZL} + I _{IL}	Off-state output current, LOW-level voltage applied		V _{CC} = MAX, V _O = 0.5 V					−70	μA
I _{OZH}	Off-state output current, HIGH-level voltage applied	ERROR	V _{CC} = MAX, V _O = 2.7 V					50	μA
I _{OZL}	Off-state output current, LOW-level voltage applied		V _{CC} = MAX, V _O = 0.5 V					−50	μA
I _{OS}	Short circuit output current ³	A0–A7	V _{CC} = MAX			−60		−150	mA
		B0–B7				−100		−225	mA
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = MAX				90	125 ⁴	mA
							90	135 ⁵	mA
		I _{CCL}					106	150 ⁴	mA
							106	160 ⁵	mA
		I _{CCZ}					98	145	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5 \text{ V}$, $T_{\text{amb}} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- For commercial range.
- For industrial range.

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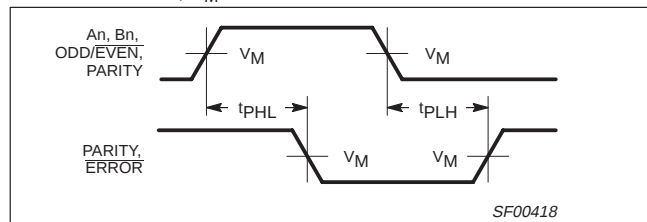
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS								UNIT
			$T_{amb} = +25\text{ }^{\circ}\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$, $R_L = 500\text{ }\Omega$			$T_{amb} = 0\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$ $V_{CC} = +5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$, $R_L = 500\text{ }\Omega$		$T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$ $V_{CC} = +5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$, $R_L = 500\text{ }\Omega$			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 2	2.5 3.0	5.5 6.0	7.5 7.5	2.5 3.0	8.0 8.0	2.0 2.5	9.0 9.0	ns	
t_{PLH} t_{PHL}	Propagation delay An to PARITY	Waveform 1, 2	7.0 7.0	10.0 10.0	14.0 15.0	7.0 7.0	16.0 16.0	5.5 6.5	16.5 19.0	ns	
t_{PLH} t_{PHL}	Propagation delay ODD/EVEN to PARITY, ERROR	Waveform 1, 2	4.5 4.5	7.5 8.0	11.0 11.5	4.5 4.5	12.0 12.5	3.5 4.0	13.0 15.5	ns	
t_{PLH} t_{PHL}	Propagation delay Bn to ERROR	Waveform 1, 2	8.0 8.0	14.0 14.0	20.5 20.5	7.5 7.5	22.5 22.5	7.5 7.5	24.5 25.0	ns	
t_{PLH} t_{PHL}	Propagation delay PARITY to ERROR	Waveform 1, 2	8.0 8.0	11.5 12.0	15.5 15.5	7.5 8.0	16.5 17.0	6.5 6.5	18.5 20.0	ns	
t_{PZH} t_{PZL}	Output enable time ¹ to HIGH or LOW level	Waveform 3, 4	3.0 4.0	5.5 7.0	8.0 9.5	3.0 4.0	9.0 11.0	2.0 4.0	9.0 13.0	ns	
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level	Waveform 3, 4	2.0 2.0	4.5 4.0	7.5 6.0	2.0 2.0	8.0 6.5	1.0 1.0	8.0 7.5	ns	

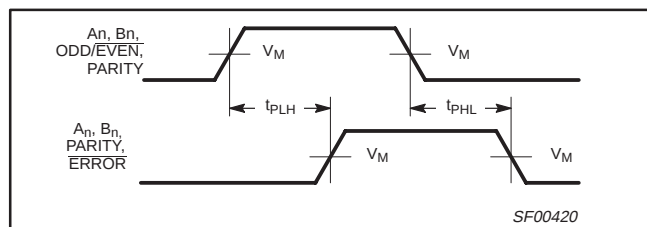
NOTE:

1. These delay times reflect the 3-state recovery time only and not the signal through the buffers or the parity check circuitry. To assure **VALID** information at the **ERROR** pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the **ERROR** output. **VALID** data at the **ERROR** pin $\geq (B \text{ to } A) + (A \text{ to } \text{PARITY})$.

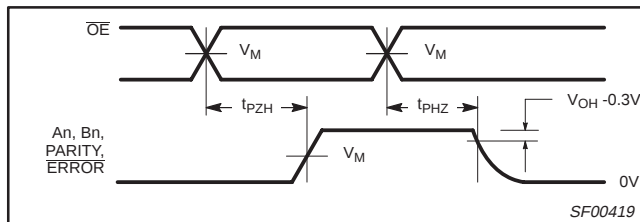
AC WAVEFORMS

For all waveforms, $V_M = 1.5\text{ V}$.

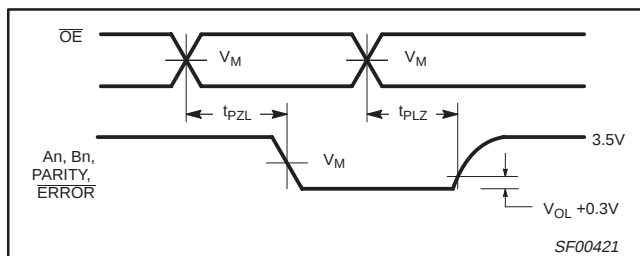
Waveform 1. Propagation delay for inverting outputs



Waveform 2. Propagation delay for non-inverting outputs



Waveform 3. 3-state output enable time to HIGH level and output disable time from HIGH level

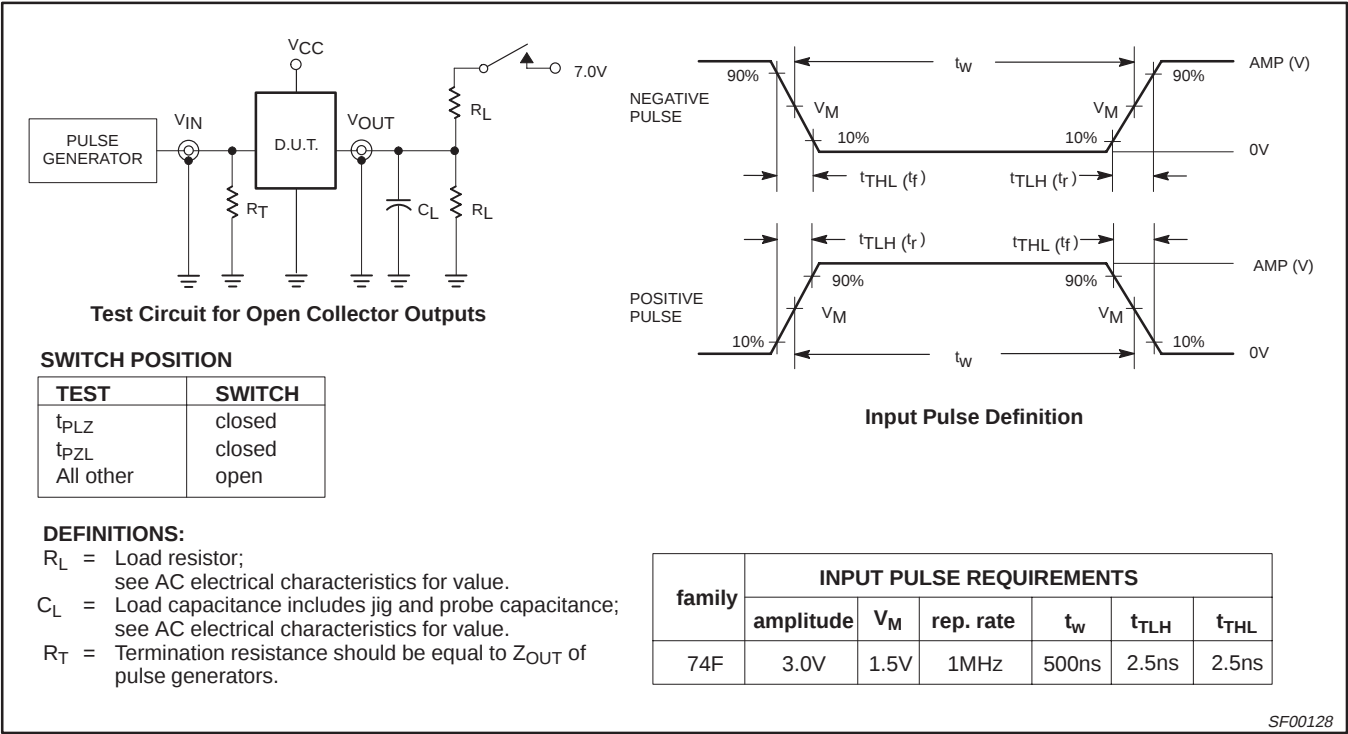


Waveform 4. 3-state output enable time to LOW level and output disable time from LOW level

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TEST CIRCUIT AND WAVEFORMS



SF00128

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DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1

Technical drawing of the SOT222-1 package showing top, side, and end views with dimensions A, A1, A2, b, b1, c, D, E, e, e1, L, ME, MH, w, Z.

0 5 10 mm
scale

DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.25	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.246	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

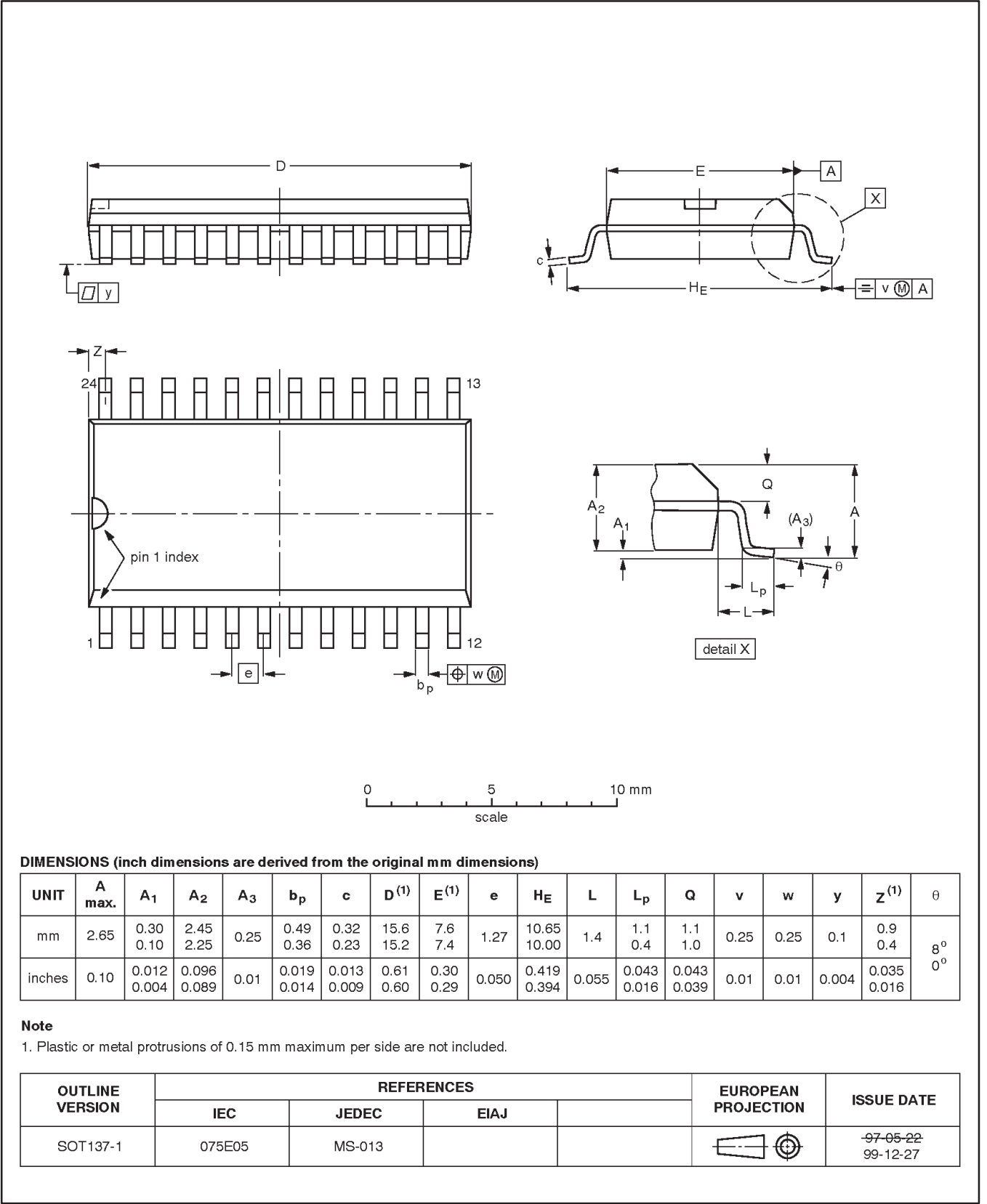
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001				99-04-28 99-12-27

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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



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REVISION HISTORY

Rev	Date	Description
_3	20030204	Product data (9397 750 11038); ECN 853-1117 29307 of 17 December 2002. Supersedes Product specification of 1990 Jul 30. Modifications: • Delete all references to DB (SSOP24) package; package option discontinued.
_2	19900730	Product specification (9397 750 05171); ECN 853-1117 00081 of 30 July 1990.

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Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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